Notice of Allowability	Application No.	Applicant(s)	
	10/015,972	ROACH, STEVEN D.	
	Examiner	Art Unit	
	Carol S. Tsai	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *2/10/2005*.

2. ☒ The allowed claim(s) is/are *17-25 and 37-42, now renumbered as 1-15*.

3. ☒ The drawings filed on *01 November 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Hong S. Lin on April 1, 2005.

The application has been amended as follows:

The application has been amended as follows:

IN THE CLAIMS:

Claims 26-35 have been canceled.

Allowable Subject Matter

2. Claims 17-25 and 37-42 are allowed.

3. The following is an examiner's statement of reasons for allowance:

U. S. Patent No. 4,222,127 to Fukaya et al. is the reference closest to the claimed invention. Fukaya et al. disclose a circuit for determining a current supplied by an integrated circuit comprising: determining a first voltage drop across a termination impedance with respect to a reference voltage; comparing a second voltage drop across a first impedance on the

integrated circuit with a third voltage drop across a second impedance on the integrated circuit, wherein the first impedance is different from the second impedance; and processing information obtained in the determining and comparing steps, wherein the information is based on the first, second, and third voltages, to obtain a value for the supplied current. However, Fukaya et al. do not teach a sensing impedance disposed on the integrated circuit; and a modulation impedance; a first measurement device coupled to the modulation and sensing impedances and configured to measure a first voltage drop across a termination impedance; a termination impedance a second measurement device coupled to the termination impedance and configured to measure a second voltage drop across the termination impedance; and processing circuitry configured to receive the first and second voltage drops measured by the first and second measurement devices, respectively, and to calculate supplied current therefrom; and including all of the other limitations in the respective independent claims.

U. S. Patent No. 4,222,127 to Fukaya et al. is the reference closest to the claimed invention. Fukaya et al. disclose a method for determining a current supplied by an integrated circuit comprising: determining a first voltage drop across a termination impedance with respect to a reference voltage; comparing a second voltage drop across a first impedance on the integrated circuit with a third voltage drop across a second impedance on the integrated circuit, wherein the first impedance is different from the second impedance; and processing information obtained in the determining and comparing steps, wherein the information is based on the first, second, and third voltages, to obtain a value for the supplied current. However, Fukaya et al. do not teach calculating a first value by dividing the value of the second impedance by the value of the first impedance, calculating a second value by dividing the value of the voltage drop across

the termination impedance by the value of the reference voltage, calculating a third value by dividing the value of the reference voltage by the value of the termination impedance, calculating a fourth value by dividing the value of the voltage drop across the first impedance by the value of the reference voltage, calculating a fifth value by dividing the value of the voltage drop across the second impedance by the value of the reference voltage, and wherein the comparing further comprises calculating a sixth value by dividing the voltage drop across the first impedance by the voltage drop across the second impedance; and including all of the other limitations in the respective independent claims.

U. S. Patent No. 4,222,127 to Fukaya et al. is the reference closest to the claimed invention. Fukaya et al. disclose a method for determining a current supplied by an integrated circuit comprising: determining a first voltage drop across a termination impedance with respect to a reference voltage; comparing a second voltage drop across a first impedance on the integrated circuit with a third voltage drop across a second impedance on the integrated circuit, wherein the first impedance is different from the second impedance; and processing information obtained in the determining and comparing steps, wherein the information is based on the first, second, and third voltages, to obtain a value for the supplied current. However, Fukaya et al. do not teach an off-chip impedance, not disposed on the integrated circuit, having a known resistance; a source impedance disposed on the integrated circuit, wherein a first terminal of the source impedance is coupled to a first terminal of the off-chip impedance; a modulation impedance disposed on the integrated circuit, wherein a second terminal of the modulation impedance is coupled to a second terminal of the off-chip impedance; a first measurement device for measuring an off-chip voltage drop across the off-chip impedance with respect to a reference

voltage; a second measurement device a source voltage drop across the source impedance with respect to a modulation voltage drop across the modulation impedance; and processing circuitry configured to determine the bias current based on the measurements of for measuring the first and Second measurement devices; and including all of the other limitations in the respective independent claims.

U. S. Patent No. 4,222,127 to Fukaya et al. is the reference closest to the claimed invention. Fukaya et al. disclose a method for determining a current supplied by an integrated circuit comprising: determining a first voltage drop across a termination impedance with respect to a reference voltage; comparing a second voltage drop across a first impedance on the integrated circuit with a third voltage drop across a second impedance on the integrated circuit, wherein the first impedance is different from the second impedance; and processing information obtained in the determining and comparing steps, wherein the information is based on the first, second, and third voltages, to obtain a value for the supplied current. However, Fukaya et al. do not teach a method for controlling the amount of output power provided by an integrated circuit, the method comprising: measuring a first voltage drop across an off-chip impedance with respect to a reference voltage, wherein the off-chip impedance is not disposed on the integrated circuit, and the off-chip impedance has a known resistance; measuring a second voltage drop across a source impedance with respect to a third voltage drop across a modulation impedance, wherein the source and modulation impedances are disposed on the integrated circuit; determining a bias current based on the first, second and third voltage measurements; and adjusting the bias current based on the determined bias current to control the amount of output power provided by the integrated circuit.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carol S. W. Tsai whose telephone number is (571) 272-2224. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571) 272-2216. The fax number for TC 2800 is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2800 receptionist whose telephone number is (571) 272-1585 or (571) 272-2800.

In order to reduce pendency and avoid potential delays, Group 2800 is encouraging FAXing of responses to Office actions directly into the Group at (703) 872-9306. This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the

examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2800 will be promptly forwarded to the examiner.

Carol S. W. Tsai
Primary Examiner
Art Unit 2857

04/01/05